IN THE CLAIMS

Please amend the claims to read as follows:

Listing of Claims

1. (Canceled).

2. (Canceled).

3. (Original) A semiconductor chip comprising a semiconductor substrate which has a top surface on which elements are integrally formed, a rear surface which opposes to said top surface in a parallel manner, an inclined plane formed so that said top surface and the inclined plane form an acute angle and a recess which is created around said top surface and which continues to said inclined plane, wherein the semiconductor chip comprises a first electrode formed on said top surface, a second electrode formed on said rear surface and a conductive pattern which is formed within said recess and on said inclined plane and which is for connecting said first electrode and said second electrode.

4. (Original) A semiconductor chip comprising a semiconductor substrate which has a top surface on which elements are integrally formed, a rear surface which opposes to said top surface in a parallel manner, an inclined plane formed so that said top surface and the inclined plane form an acute angle and a recess which is created around said top surface and which continues to said inclined plane and has a surface electrode which is connected to said elements, wherein the semiconductor chip comprises a first insulating layer formed on the inside walls of said recess and on said top surface other than on said surface electrode, a first conductive pattern which is filled into said recess where said first insulating layer is formed and which is formed on said top surface where said first insulating layer is formed in a desired wire and electrode form so as to be connected to said surface electrode, a second insulating layer formed on said top surface with openings for an electrode part made of said first conductive pattern, an inclined part where said first conductive pattern in said recess is exposed so as to continue to said inclined plane around said rear surface, a third insulating layer formed on said rear surface and on said inclined plane with an opening for said inclined part from which said first conductive pattern is exposed, a second conductive pattern

which is formed on said inclined plane where said third insulating layer is formed and on the rear surface of said semiconductor chip in a desired wire and electrode form so as to be connected to said first conductive pattern and a fourth insulating layer formed on the rear surface and on said inclined plane of said semiconductor chip with an opening for an electrode part made of said second conductive pattern.

5. (Canceled).

6. (Canceled).

7. (Canceled).

8. (Canceled).

9. (Currently Amended) A wiring board of which the base material is silicon, characterized in that a plurality of through holes are created in said wiring board, a first conductive pattern is formed on a surface of said wiring board, said through holes are created in an inclined plane formed so that the inner angle made up of ~~the~~ a rear surface of said wiring board and the

inclined plane is an obtuse angle, a second conductive pattern is formed on said rear surface and on said inclined plane and said first conductive pattern and said second conductive pattern are electrically connected through a third conductive pattern formed in said plurality of through holes.

10. (Original) A wiring board for a multi-chip semiconductor device on which electronic parts are mounted and which is mounted on a mother board, characterized in that said wiring board has a silicon substrate made of silicon, in that a first conductive pattern for mounting and wiring said electronic parts which is made of, at least, one layer is provided on a top surface of this silicon substrate and a second conductive pattern made of, at least, one layer which has an electrode for being mounted on said mother board is provided on a rear surface of said silicon substrate and in that said first conductive pattern and said second conductive pattern are electrically connected through a third conductive pattern formed on a side surface of said silicon substrate.

11. (Original) A wiring board for a multi-chip semiconductor device on which electronic parts are mounted and

which is mounted on a mother board, wherein said wiring board is characterized by comprising a silicon substrate made of silicon wherein a side surface is formed so that a top surface and the side surface of the substrate form an acute angle while a recess is formed around the substrate, a first conductive pattern made of, at least, one layer having an electrode formed on the surface and within said recess of said silicon substrate and a second conductive pattern made of, at least, one layer having an electrode which is formed on the rear surface and on said side surface of said silicon substrate and which is connected to said first conductive pattern.

12. (Previously Presented) A wiring board according to Claim 9, wherein an insulating layer is formed on a side surface so that the surface of the insulating layer and the surface of the substrate form a right angle.

13. (Previously Presented) A wiring board according to Claim 9, comprising a resin layer of low stress inserted either between the first conductive pattern and the substrate or between the second conductive pattern and the substrate or inserted in both cases.

14-29. (Canceled).

30. (Original) A semiconductor device, characterized in that a plurality of semiconductor chips, comprising semiconductor substrates, first external electrodes formed on first surfaces of said semiconductor substrates, second external electrodes formed on second surfaces of said semiconductor substrates and through holes created in said semiconductor substrates, wherein said through holes are created in inclined planes formed so that the internal angles made up of said second surfaces and the inclined planes are obtuse angles and said first external electrodes and said second external electrodes are electrically connected through conductive patterns formed so as to follow the inner walls of said through holes and said inclined planes, are layered while said respective first external electrodes and said respective second external electrodes are electrically connected.

31. (Original) A semiconductor device characterized in that between two first semiconductor chips comprising semiconductor substrates, first external electrodes formed on first surfaces of said semiconductor substrates, second external electrodes formed on second surfaces of said semiconductor substrates and through

holes created in said semiconductor substrates, wherein said through holes are created in inclined planes formed so that the internal angles made up of said second surfaces and the inclined planes are obtuse angles and said first external electrodes and said second external electrodes are electrically connected through first conductive patterns formed so as to follow the inner walls of said through holes and said inclined planes, a second semiconductor chip wherein third external electrodes formed in the parts other than the region of the third surface on which elements are formed and fourth external electrodes formed in the parts other than the region of the fourth surface on which elements are formed are electrically connected through second conductive patterns is provided so that said first semiconductor chips and said second semiconductor chip are electrically connected directly or via connection members.

32. (Original) A multi-chip type semiconductor device formed by layering a plurality of semiconductor chips comprising semiconductor substrates with top surfaces on which elements are integrally formed, wherein said layered semiconductor chips comprise semiconductor substrates having said top surfaces, rear surfaces which are opposed to said top surfaces in a parallel

manner, inclined planes formed so that the inclined planes and said top surfaces form acute angles and recesses created in the periphery around said top surfaces and comprise first external electrodes formed on said top surfaces, second external electrodes formed on said rear surfaces and conductive patterns formed in said recesses and on said side surfaces for connecting said first external electrodes and said second external electrodes and wherein said semiconductor chips are electrically connected to other semiconductor chips via said first external electrodes and said second external electrodes.

33. (Original) A semiconductor device according to Claim 32, wherein the layered semiconductor chips are electrically connected to other semiconductor chips directly above and directly below said semiconductor chips by directly connecting the electrodes thereof or via connection members.

34. (Previously Presented) A wiring board according to Claim 11, wherein an insulating layer is formed on a side surface so that the surface of the insulating layer and the surface of the substrate form a right angle.

35. (Previously Presented) A wiring board according to Claim 10, comprising a resin layer of low stress inserted either between the first conductive pattern and the substrate or between the second conductive pattern and the substrate or inserted in both cases.

36. (Previously Presented) A wiring board according to Claim 11, comprising a resin layer of low stress inserted either between the first conductive pattern and the substrate or between the second conductive pattern and the substrate or inserted in both cases.

37-48. (Canceled).